PCIe® 4.0 Compliance Update

David Bouse

SEG Member

Intel Corporation

Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

PCIe® 4.0 Compliance Program Status

PCI Express® 4.0 Time Frames

Test Specifications

- Config Test Specification – Rev 0.5 Work Group Approved
- Link/Transaction Test Specification – Rev 0.5 Work Group Approved
- System Firmware (BIOS) Test Specification – Rev 0.7 Work Group Approved
- Electrical Test Specification – Rev 0.5 Work Group Approved
  - Rev 0.7 work nearing completion
- Retimer Test Specification – 0.5 Work Group Approved

Integrator's List

- Pre-FYI testing was done in January 2017 and will continue until official FYI status is reached
- FYI testing targeting late 2018
- Official testing targeting middle 2019

PCIe 4.0 Config, Link/Transaction, & BIOS Test Status

PCIe 4.0
Config, Link/Transaction, & Bios Tests

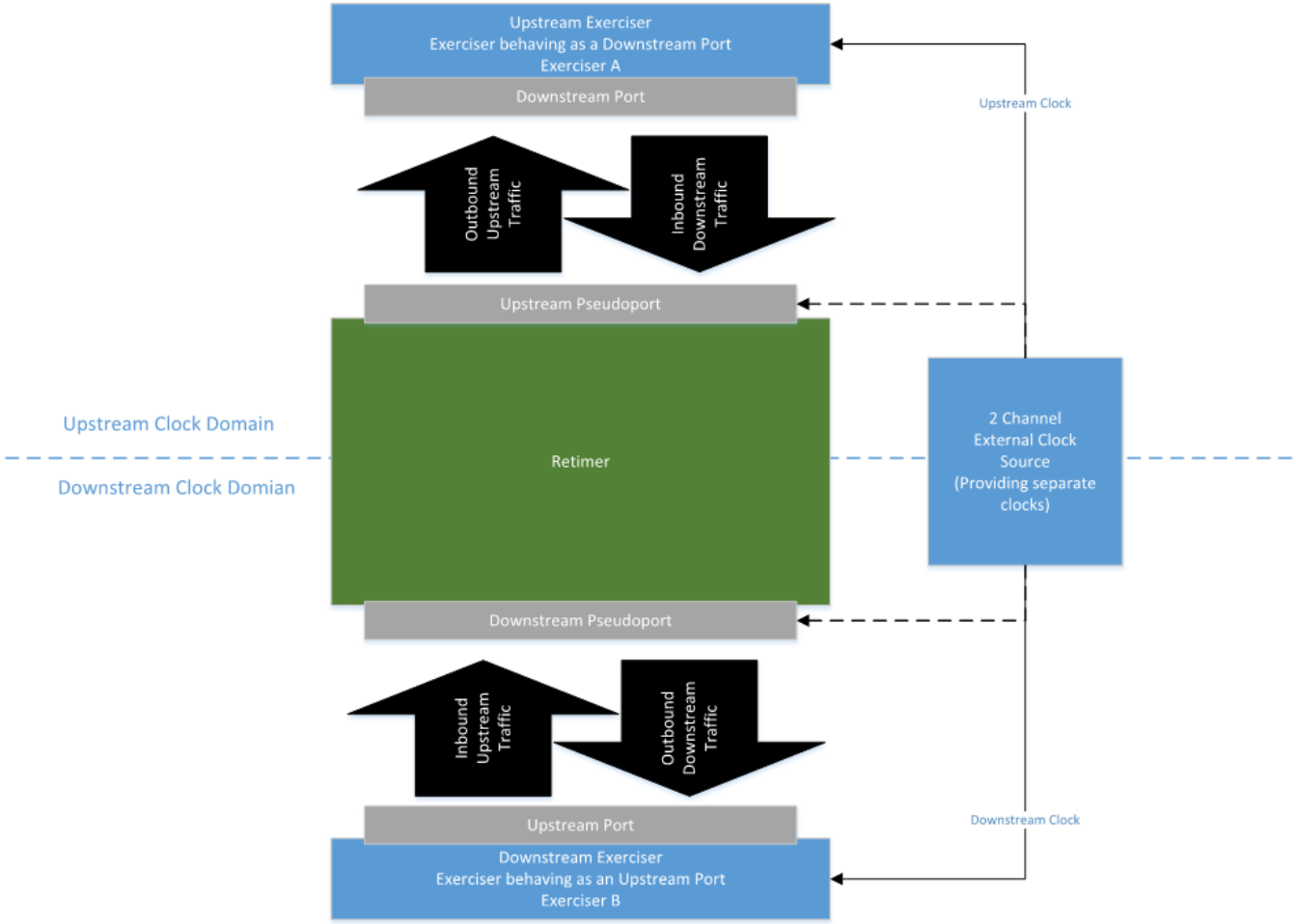
- **PCIe 4.0 Config Tests**
  - Currently 4.0 devices are being tested using 3.0 CV software
  - Preliminary FYI began at Compliance Workshop #105 (April 2018)
    - Performed with 3.0 system at 8 GT/s
  - CV 4.0 software is expected to be at 10-20% functionality for workshop #106
  - Final version of CV 4.0 software targeting Q4 2018
- **Link/Transaction Tests**
  - Currently preliminary FYI is happening for 4.0 (Add-in Card's only)
  - System testing is still under development
- **Bios Tests**
  - Currently no testing available
  - PCI-SIG is working with the TE tool providers to develop hardware/software capable of performing the 4.0 BIOS test & System Link/Transaction testing

PCIe 4.0 Retimer Test Status

PCIe 4.0
Retimer Compliance Status

- **Serial Enabling Group (SEG)**
  - Ad-Hoc Retimer workgroup developing Rev 0.7 test specification
    - Sean Stalley (Intel)
  - Retimer testing has not started at compliance workshops
- **Electrical Tests**
  - Same as PCIe 4.0 Base Electrical Tests
    - Tx Voltage & Jitter measurements with breakout board
    - Rx Tests performed with PCIe 4.0 Base Rx Calibration fixtures
- **Forwarding Mode Tests**
  - Logical & timing test performed when the retimer under test is forwarding traffic between the upstream & downstream ports
  - Ad-Hoc group is currently focused on development of forwarding mode tests
- **Execution Mode Tests**
  - Logical & timing tests performed when the retimer forms two separate electrical links between the upstream port and the downstream port
  - Development of execution mode tests will begin after forwarding mode test are completed

PCIe 4.0
Retimer Forwarding & Execution Setup

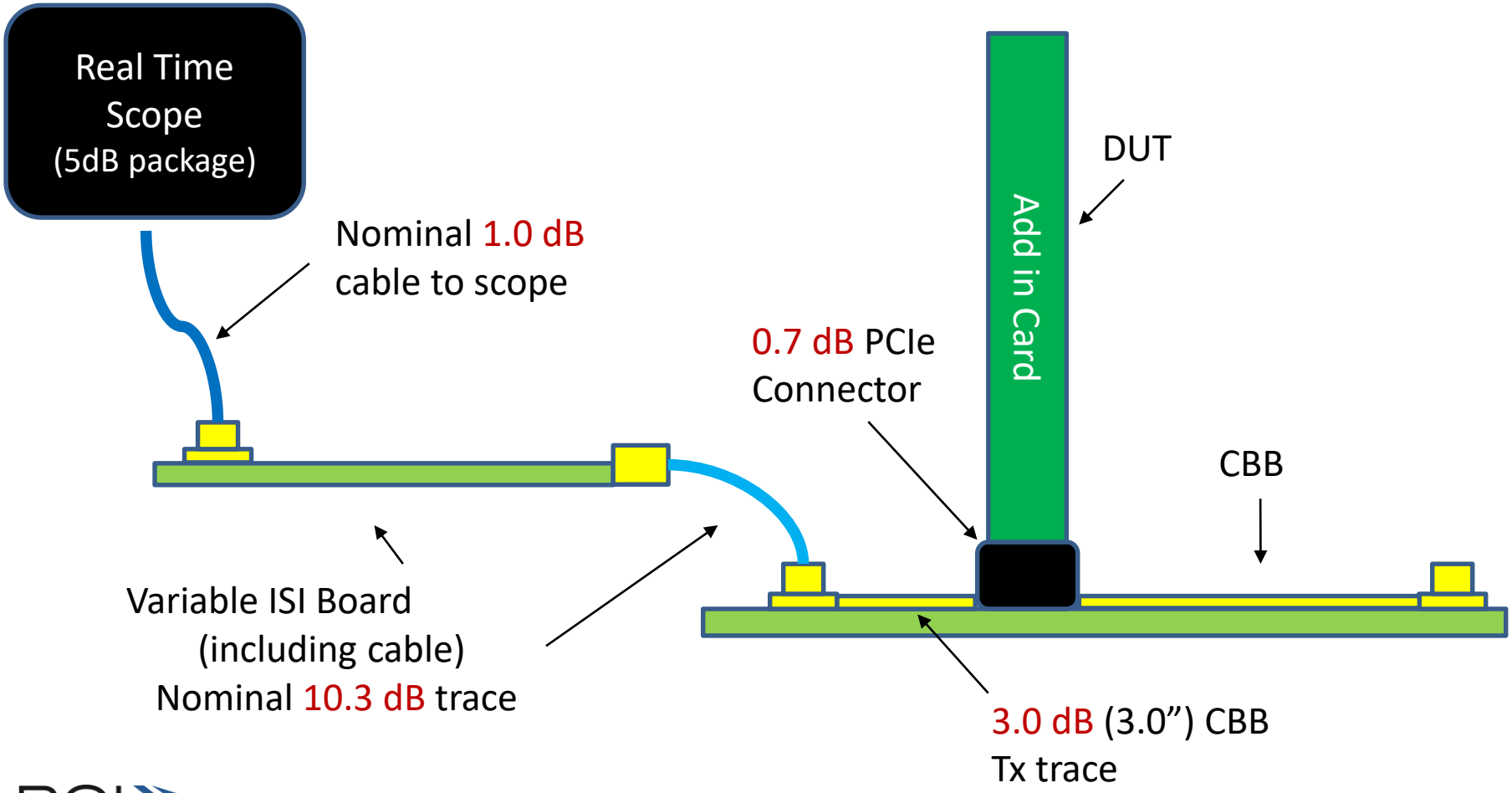


PCIe 4.0 Electrical Tests

PCIe 4.0
Electrical Tests Under Development

- **Transmitter (Tx) Signal Quality Test at 16 GT/s**
  - End of channel eye diagram (eye width & eye height)
- **Tx Preset Equalization Test at 16 GT/s**
  - Measures voltage levels for Preset 0 to Preset 10
- **Tx Pulse Width Jitter at 16 GT/s (Add-in Card)**
  - Clock pattern used to measure the Base Spec Pulse Width Jitter limit
- **PLL Bandwidth (Add-in Card)**
  - Verifies an Add-in Card's PLL bandwidth & peaking
- **Link Equalization Handshaking at 16 GT/s**
  - Confirms Tx starts with correct preset requested through protocol
  - Tx responds to protocol changes and adjusts voltage levels
  - Receiver (Rx) correctly adjusts the link Tx and operates with a stressed eye
- **All 2.5/5.0/8.0 GT/s Testing Still Required for 4.0 Integrators List for a 16GT/s Capable Devices**

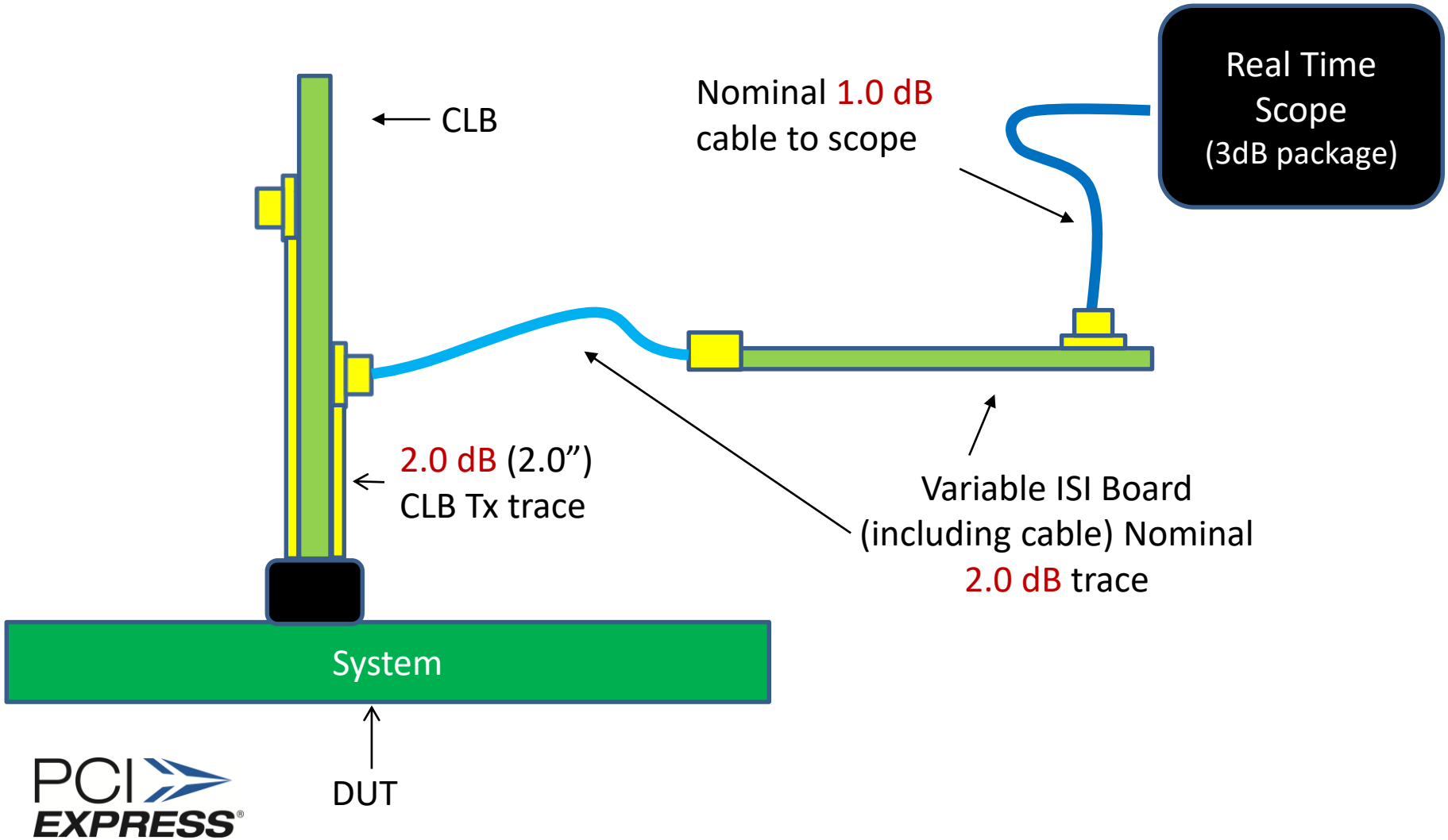
PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s



PCIe 4.0 (Add-in Card)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB -> Variable ISI Board -> Scope
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope Bandwidth is 25GHz**
- **5dB Package Model Embedded on Scope**
- **Toggle DUT to Transmit 16 GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI Waveform for every Tx EQ Preset**
- **Waveforms Post Processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 24.75 ps
    - EH > 23 mV

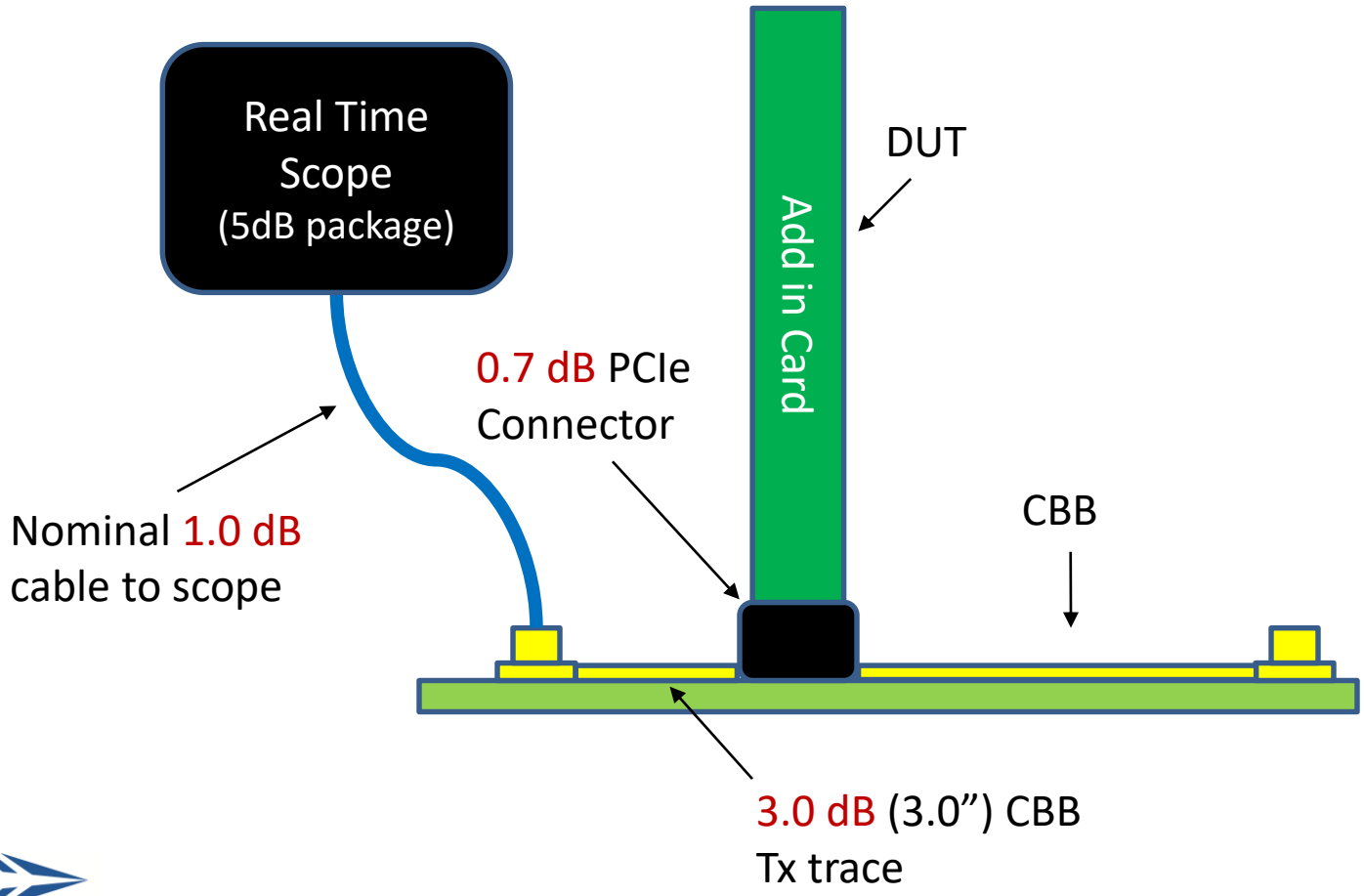
PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s



PCIe 4.0 (System)
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system -> Variable ISI Board -> Scope
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope Bandwidth = 25GHz**
- **3dB Package Model Embedded on Scope**
- **Toggle DUT to Transmit 16 GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI Waveform for Every Tx EQ Preset**
- **Waveforms Post Processed Using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 21.75 ps
    - EH > 19 mV

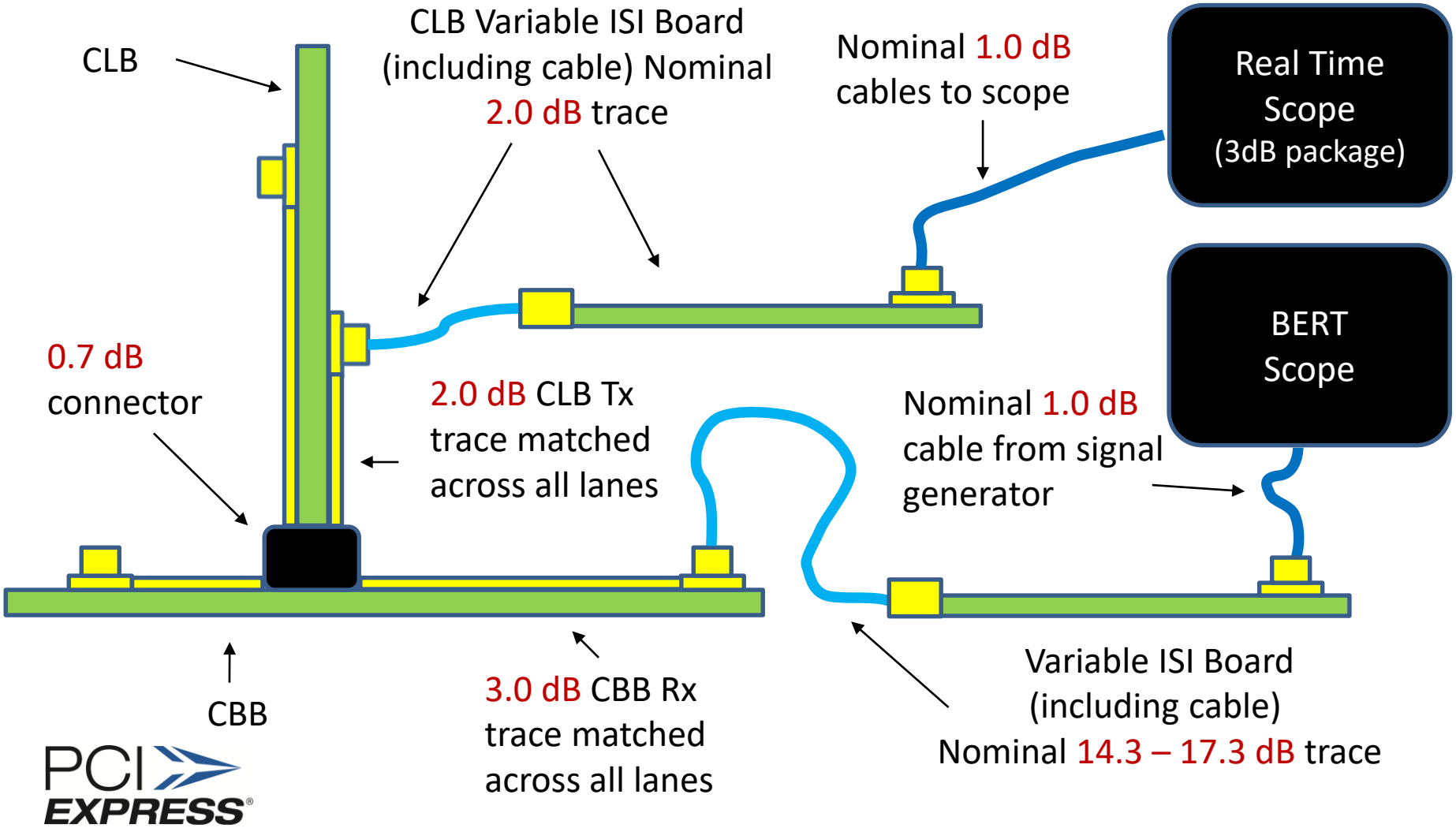
PCIe 4.0 (Add-in Card)
Tx Pulse Width Jitter at 16 GT/s



PCIe 4.0 (Add-in Card)
Tx Pulse Width Jitter at 16 GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB -> Scope
  - Only adding CBB & cable loss (no package embedding)
- **Power on CBB**
- **Scope Bandwidth is 25GHz**
- **No Package Embedding on the Scope**
- **Toggle DUT to Transmit 16 GT/s Clock Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI Waveform for Every Tx EQ Preset**
- **Waveforms Post Processed Using SigTest**
  - SigTest Base Rx Mode
  - PWJ Tj @ E-12 (ps) value is recorded
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - PWJ <= 12.5 ps

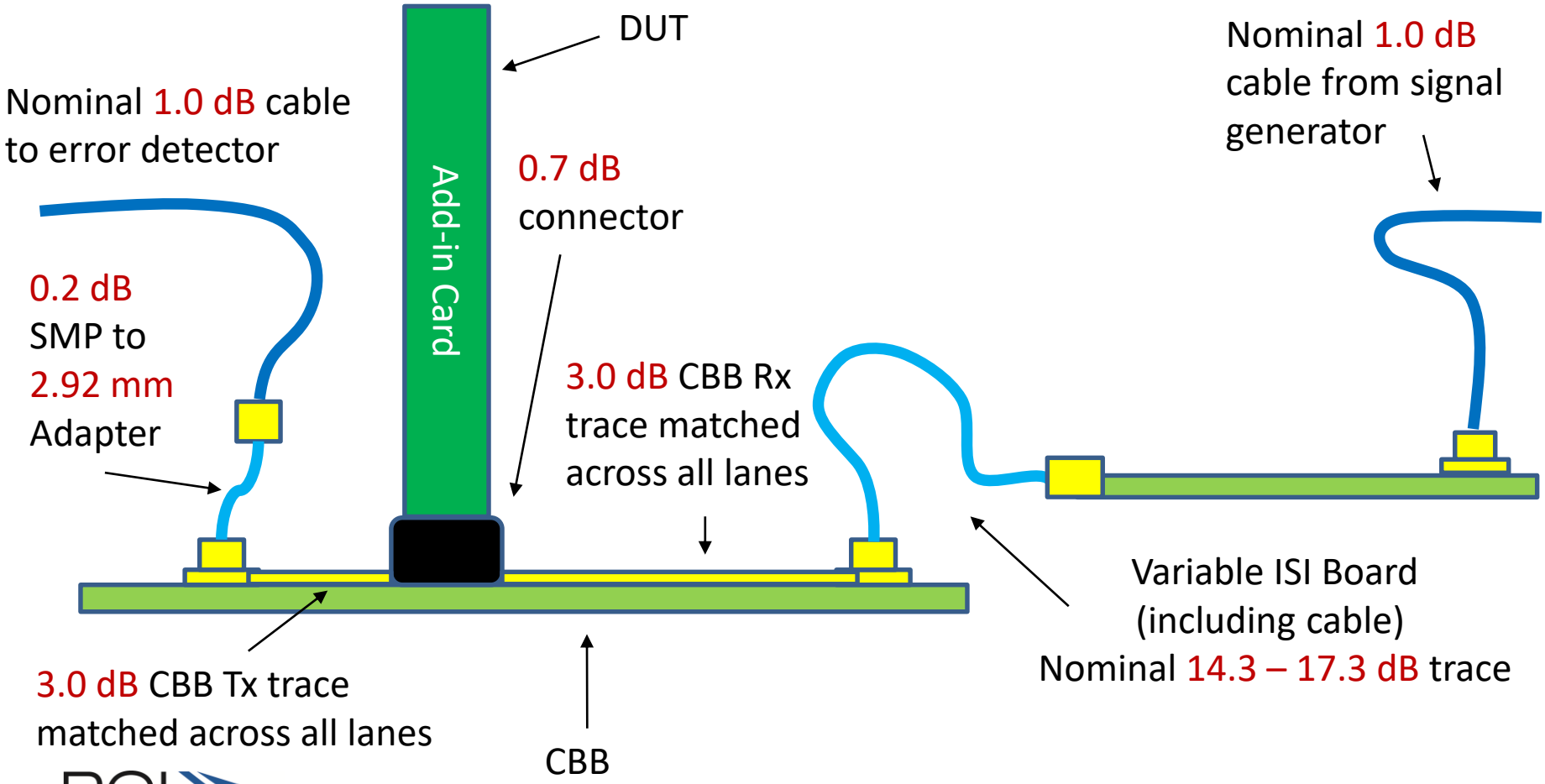
PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16GT/s



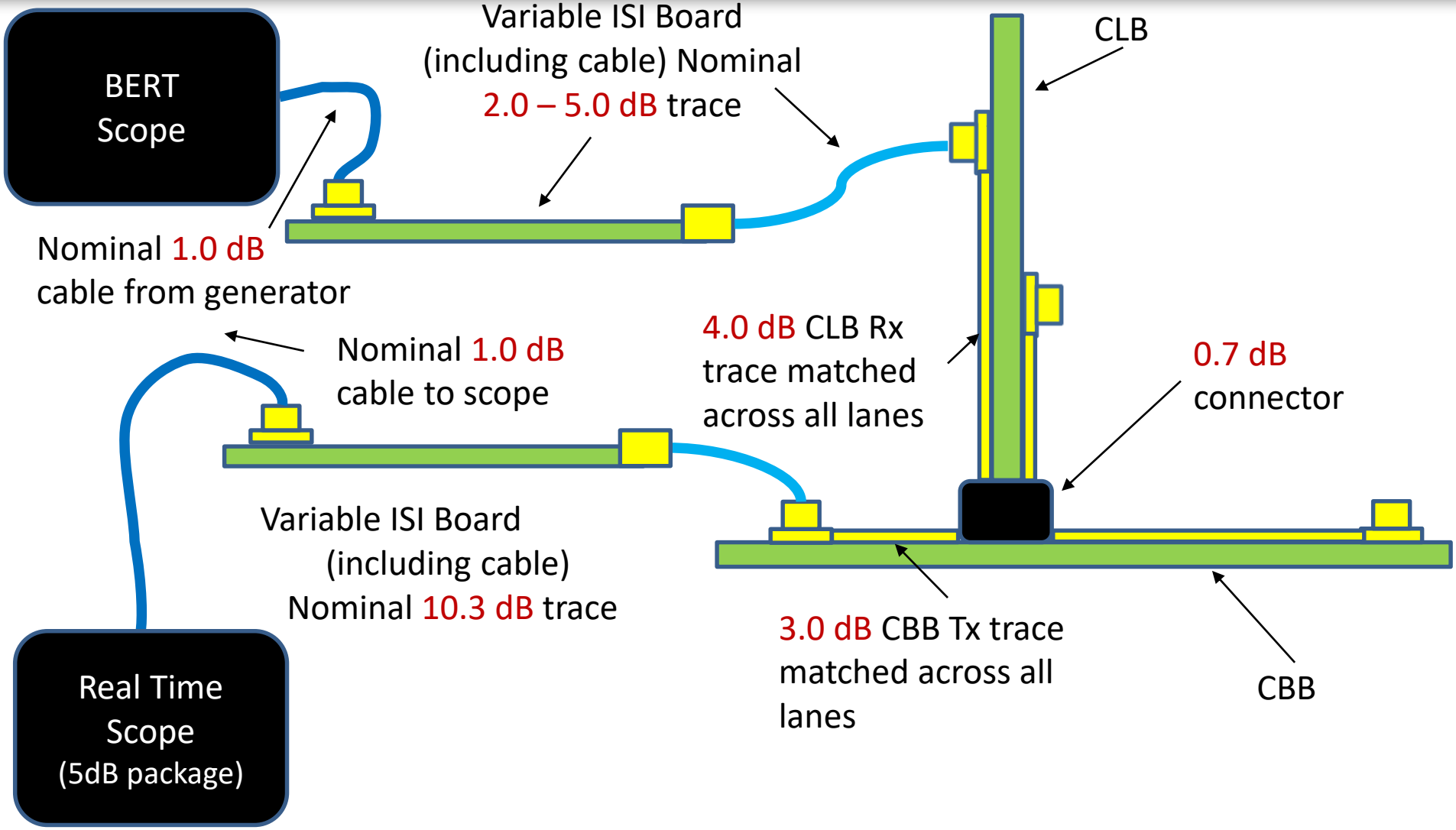
PCIe 4.0 (Add-in Card)
Rx Stressed Eye Calibration at 16 GT/s

- **Calibrate Swing & Tx EQ Presets**
  - Setup - SMA cable from BERT to Scope
  - Swing calibrated to 800mV differential
  - Calibrate voltage levels for Preset 0 - 9
- **Calibrate Rj & Sj**
  - Setup - SMA cable from BERT to Scope
  - Rj – 1ps RMS (clock pattern used)
  - Sj – 0.1UI (PCIe 4.0 compliance pattern used)
- **Channel Setup**
  - BERT -> Variable ISI -> CBB -> CLB -> Variable ISI -> Scope
  - 27 – 30dB at 8GHz of additional loss (including 3dB package embedding)
- **Calibrate DMI & CMI**
  - DMI – 14mV (End of 27dB Channel)
  - CMI – 150mV (End of 27dB Channel)
- **Channel Selection**
  - Increase channel loss from 27 to 30dB
  - Find channel where the eye width/height is closest to target without dropping below
    - Must use Optimal Tx EQ Preset which is the Preset which gives the largest eye area
- **Eye Width & Eye Height Calibration**
  - Optimal Tx EQ Preset is used with final channel
  - Adjust Sj (5-10ps), DMI (10-25mV), & Swing (720-800mV) until eye width/height (measured with SigTest) targets are achieved
  - EW = 18.75 +/- 0.5ps EH = 15mV +/-1.5mV

PCIe 4.0 (Add-in Card)
Rx Stressed Eye Test at 16 GT/s



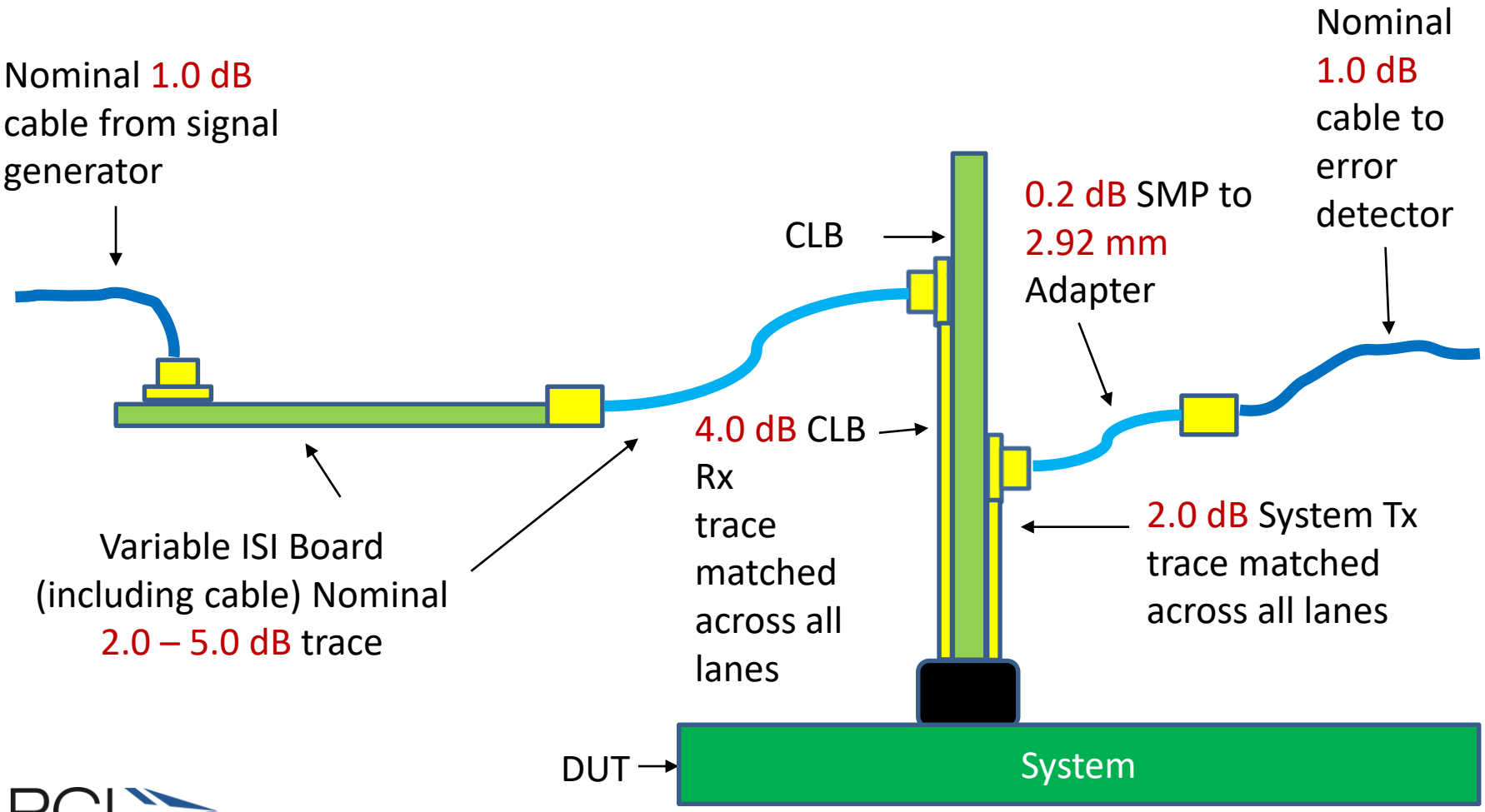
PCIe 4.0 (System)
Rx Stressed Eye Calibration at 16 GT/s



PCIe 4.0 (System)
Rx Stressed Eye Calibration at 16 GT/s

- **Calibrate Swing & Tx EQ Presets**
  - Setup - SMA cable from BERT to Scope
  - Swing calibrated to 800mV differential
  - Calibrate voltage levels for Preset 0 - 9
- **Calibrate Rj & Sj**
  - Setup - SMA cable from BERT to Scope
  - Rj – 1ps RMS (clock pattern used)
  - Sj – 0.1UI (PCIe 4.0 compliance pattern used)
- **Channel Setup**
  - BERT -> Variable ISI -> CLB -> CBB -> Variable ISI -> Scope
  - 27 – 30dB at 8GHz of additional loss (including 5dB package embedding)
- **Calibrate DMI & CMI**
  - DMI – 14mV (End of 27dB Channel)
  - CMI – 150mV (End of 27dB Channel)
- **Channel Selection**
  - Increase channel loss from 27 to 30dB
  - Find channel where the eye width/height is closest to target without dropping below
    - Must use Optimal Tx EQ Preset which is the Preset which gives the largest eye area
- **Eye Width & Eye Height Calibration**
  - Optimal Tx EQ Preset is used with final channel
  - Adjust Sj (5-10ps), DMI (10-25mV), & Swing (720-800mV) until eye width/height (measured with SigTest) targets are achieved
  - EW = 18.75 +/- 0.5ps EH = 15mV +/-1.5mV

PCIe 4.0 (System)
Rx Stressed Eye Test at 16 GT/s



Link Equalization Tests

- **Tests Required for 8 GT/s & 16 GT/s**
- **Requires protocol-aware test equipment**
  - Anritsu, Keysight, & Tektronix BERTs all support Link Equalization Testing
- **Tx link equalization response test**
  - Use protocol-aware test equipment to request a Tx equalization change
  - Check that the DUT responds and sets its Tx to the correct preset within required time period
  - Measurement of DUT Tx done by going to loopback and sending compliance pattern
  - Do this check for all presets
- **Rx link equalization**
  - Calibration the same as standard Rx test
  - Start with a non-optimal Tx equalization setting (P7 or P8)
  - Allow DUT to request for equalization adjustments
  - Place DUT into loopback
  - Monitor bit stream for errors

Add-in Card PLL Bandwidth

- **Test Required for all supported data rates up to 16 GT/s**
  - Verifies that the Add-in card PLL bandwidth is within the limits allowed by the PCIe specification
- **Test requires a reference clock generator capable of adding phase jitter from 0 to 25 MHz**
  - Anritsu, Keysight, LeCroy, and Tektronix all have capable generators
- **Test steps**
  - Insert Add-in card into CBB & connect the toggle signal to Rx Lane 0
  - Connect the output of transmit lane 0 on the CBB to an instrument capable of measuring the transmitter frequency response as a function of phase jitter on the reference clock
  - Power on the CBB with the DUT in place
  - Apply modulation on the reference clock from 0 to 25 MHz ensuring the phase jitter is within 20% of the limit allowed by the PCIe specification
  - Measure the transmitter output on lane 0 across this range and estimate the -3dB point. Also note the maximum amplitude of the transmitter
  - The – 3dB point must fall between the frequencies specified for each data rate and the maximum peaking must be less than that allowed for each data rate
  - Repeat these steps with the amplitude set to ½ of the initial calibrated values
  - A passing result with any preset is acceptable

Compliance Program Overview

- **PCIe 4.0 Test Program Under Development**
- **PCIe 3.0 Integrators List testing (started April 2013)**
  - Tests for 2.5, 5, 8 GT/s maximum data rates
- **Card Electromechanical (CEM) form factor only**
- **Other form factors**
  - FYI testing underway for SFF-8639/U.2
  - M.2 (Socket 3) under development
- **PCI™, PCI-X™, PCIe 1.x, PCIe 2.0 retired as of October, 2017**
  - PCIe 3.0 testing continues, along with 4.0 preliminary FYI testing
  - 2.5 and 5 GT/s testing will continue as part of 3.0/4.0 process
- **Usually announced 2 months in advance**
  - Registration ends 3 week prior for domestic and 4 weeks for international
  - No on-site registration!!!!
- **Passing at a workshop is the only way to be listed on the PCI-SIG Integrators List**
  - Pass all gold suite tests
  - Pass interoperability testing

Thank you for attending the PCI-SIG Developers Conference 2018.

For more information, please go to www.pcisig.com

Don't forget to submit your feedback via the mobile app!

Download the **Crowd Compass** app and then search for **PCI-SIG Developers Conference** or entering the following URL into your mobile browser: https://crowd.cc/s/1rKy0
Enter event code: **DevCon2018**

Alternatively, access here: https://crowd.cc/pcisig2018

Note: Create an account within the app so Admin knows who to contact if selected as the prize winner.

Each session feedback is provided is equivalent to 1 raffle entry (up to 11 sessions).
General survey feedback = 1 raffle entry.